EE2007.8 Release Notes

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Contractor/manufacturer is:
Mentor Graphics Corporation
8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.
Telephone: 503.685.7000
Toll-Free Telephone: 800.592.2210
Website: www.mentor.com
SupportNet: supportnet.mentor.com/
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Chapter 1
Constraint Editor System (CES)

Problems Fixed

- **dts0100542175** — cannot delete any power net from the list
- **dts0100588014** — Resolve formulas does not highlight the cell with any violation.
- **dts0100607879** — Hierarchical Constraint Classes Do not Export and Import Correctly - Import Loses Net assignments
- **dts0100623209** — New added labels on nets in DxDesigner are not updated in CES.
- **dts0100624773** — CES: Must be able to specify Max Vias in a Constraint Template
- **dts0100625026** — CES - Constraints: Crash when attempting to apply a constraint template with netclass defined
- **dts0100625793** — Templates with length matching don't always work, inconsistent results.
- **dts0100628227** — CES Crash when appling Constraint Template
- **dts0100630835** — Creating a new scheme in CES causes a crash in Expedition
- **dts0100631382** — Problems updating and changing the layer route assignments in NETCLASSES.
- **dts0100631830** — CES - DC: Has 2 Netclasses in CES (Diff90 and Power) that don't show up in Trace and Via Properties

Chapter 2
Design Capture

Problems Fixed

- **dts0100569233** — Different syntax for inverted signals
- **dts0100596859** — Packager fails with ERROR: duplicate physical nets found... messages
- **dts0100608354** — iCDB to EDIF fails to generate file with correct data; i.e. Property Value
- **dts0100631825** — DC - iCDB Complile: Duplicate Net messages for netnames clearly in the Globals file
- **dts0100634271** — Duplicate Netname warning at compile when a part of a circuit was copied before
- **dts0100614430** — Page Admin Swap/Insert Disconnects Nets
- **dts0100631710** — Modify the schematic and then incremental compile will change pcb flatnet name of global nets and give "Duplicate net name" compiler warning

Known Problems and Workarounds

- **dts0100498140** — Help for all Design Capture dialogs doesn't work on VISTA

  Workaround: Download the WinHlp32.exe from Microsoft website and load it in Vista system.

- **dts0100446350** — Unable to upgrade the design

  Workaround: Follow the error prompts and then use the Project Settings dialog to update the path of the bus contents file before upgrading the design again.

- **dts0100575137** — After placing a new device with assigned Cell Name, the Part Number value becomes a Cell Name value on the DC schematic and this will cause the packager error

  Workaround: Invoke the Library Manager (stand-alone or from DC) to update the Central Library, then delete the part in question and place the new part with specific cell name again on the schematic.

- **dts0100575158** — New placed parts: The Part Name or Reference Designator value becomes a Cell Name value on DC schematic after Back Annotation

  Workaround: Invoke the Library Manager (stand-alone or from DC) to update the Central Library, then delete the part in question and place the new part on the schematic.

Chapter 3
DMS Librarian

Problems Fixed

- **dts0100618061**— PRM web page takes an extraordinarily long time to come up

Chapter 4
DxDesigner

Problems Fixed

- **dts0100372438** — DxPDF EXP2005.1 generates smal dots instaed of text on Solaris 8 and 9
- **dts0100495671** — Strange rounding in millimeters
- **dts0100539584** — Its not possible to rename the design name in the DXD Navigator (only 1 design)
- **dts0100541964** — DxPDF pager order does not work based on the scout SHEET order property. Please reference DR 541962.
- **dts0100549052** — Cannot use Japanese font in Symbol Editor.
- **dts0100564958** — VDRC does not create vdrc.log file if there is no "Log Files" folder i project directory.
- **dts0100575820** — DRC-201 does not work correctly
- **dts0100596003** — DC2DA and DxDesigner need to support LineStyle6-LineStyle16 from Design Capture.
- **dts0100602277** — Pin number will not be displayed if Pin Label are either lower or mix case.
- **dts0100603902** — "Add Missing ports" on an IO Designer generated schematic for DxDesigner the ports are placed outside the schematics.
- **dts0100605863** — PCBFWD: Customer can not use Arguments in "Customize Tools Menu"
- **dts0100615921** — "Un-loaded net" does not work in the case of "PIN" type symbol.
- **dts0100618179** — When placing components from DxDatabook it don not change "," comma to a "." dot as it do in 9.0PADS, this result in error when doing netlist.
- **dts0100620072** — Place Reuse Block in Schematic Hangs DxDesigner
- **dts0100622216** — DxDatabook Annotate Properties to Selected Components not working
- **dts0100622712** — The customer has an Orcad Capture schematic, which he converted to DxD. The schematics look fine, but when he generates the netlist and opens PADS Layout he finds a wrong connection (short-circuit).
- **dts0100623059** — Cannot edit Instance Value in Properties Window
- **dts0100623081** — Ref Designator value not visible in the Properties addin

- **dts0100625050** — Schematic sheet cannot be opened after updating EE2007.3 project to EE2007.5, EE2007.6 OR EE2007.7
- **dts0100625913** — DxDesigner crashes after change to ICT schematic with Reuse Block
- **dts0100625963** — Migrated DC/DV database to DxDesigner - FWDAnno reassigns; breaks back and removes huge amount of traces.
- **dts0100628692** — Error 1287: iCDB database update error: UID Manager: Object not found
- **dts0100628735** — Error 1287 when trying to delete bus segment. Diagnostics results in schematic that cannot be opened in schematic or block view.
- **dts0100629187** — DxDesigner Diagnostics does not fix the attached project.
- **dts0100630994** — "Cannot generate Schematic view. Finish or cancel previous operation" message from VM when reuse block is included in Schematic
- **dts0100631034** — DxPDF crashes if "Schematic Sheet Order Property" is used
- **dts0100631373** — Unable to Save Symbol: Error UID Manager: Object not found
- **dts0100631630** — I get Error: Schematic block 'Schematic1.1' has elements with duplicate IDs needed for Backup/Rollback and copying

Known Problems and Workarounds

- **dts0100440990** — 'Maximize button change height of DxD to half of the screen - SUSE10

  Workaround: manually resize the window

- **dts0100468973** — Packager returns errors after placing RB that contains symbols with vectored pins

  Workaround: Modify the design before migration (replacing {} with some other construct which is supported - (e.g. {DRAIN1}3 into DRAIN1, DRAIN1, DRAIN1) and then creating an RB after migrating such modified design.

- **dts0100492837** — MySQL ODBC does not work in databook on Windows Vista 64bit

  Workaround: Only Oracle 32-bit drivers can be used on Windows Vista 64 bit.

- **dts0100492879** — pcbfwd fails on a migrated Expedition netlist with Central Library (pdb) design.

  Workaround: Add all required PCB properties (#, DEVICE, PKG_TYPE) at a symbol level.

- **dts0100493259** — 'The specified Project File does not define a Central Library' when creating a new PCB project based on the DxD netlist prj

  Workaround: Create a separate project file for the Expediton PCB. DxDesigner project file cannot be used for the netlist flow.

- **dts0100500162** — Cannot open "Knowledge Base" and "Log a Support Request" from the Service & Documentation Center Toolbox

  Workaround: Go to Edit/Preferences/General , uncheck "Use the internal Dashboard Web Browser" and point another web browser (which is able to show requested page).

- **dts0100504235** — Preview window in Symbols addin does not display bitmaps in symbols.

  Workaround: Place the symbol in the schematic to see the bitmap.

- **dts0100505027** — Extract schematic - haven't got information when ports are not defined.

  Workaround: Define hierarchical ports using Setup->Settings->Special Components tab before creating blocks.

- **dts0100505900** — I can't create diff pair for unlabeled nets

  Workaround: Name the nets using the Properties window before creating a differential pair.

- **dts0100508265** — vlib: Error: Unable to parse the integer token 'ffff00' from the "string. when exporting HPGL file from DxDesigner

  Workaround: HPGL file can be generated on Windows platform.

- **dts0100509882** — DxWebPack does not work in Windows Vista as a server.

  Workaround: The path to dxdbweb.dll must be set in "ISAPI and CGI Restrictions" option on server level in IIS. Next, DxDataBook server must be configured in DxDBConfig tool. There are two tabs: "DxDB Client Access" and "Browser Access".

  "DxDB Client Access" - use this tab to choose ODBC Data Source Name and to add database aliases to chosen data source. Database aliases allow to define the set of data source names visible to DxDataBook client. After configuring this tab, it is possible to connect to DxDB Server and specified database from DxDataBook.

  "Browser Access" - use this tab of DxDBConfig to specify the database configuration file that you want to use in the web extension to DxDataBook. After selecting DBC file, all tables configured in this file will be visible in explorer. It is needed to restart the web server in IIS after configuring the DxDBConfig. After restarting, It is possible to connect to DxDB web server from DxDataBook and from explorer.

- **dts0100584265** — Cannot pass Value property from DxD to CES for an arrayed component

  Workaround: set the Value directly in CES.

- **dts0100622034** — OLD Flow is not shown for invoking ModelSim as seperate GUI with all features enabled

  Workaround: See Technote MG249765

- **dts0100622290** — External Dx-ModelSim Flow: Unable to backannotate sim values into schematic

Workaround: See Technote MG249765

Chapter 5
Expedition PCB

Problems Fixed

- **dts0100422233** — ODB++, rotates and outputs the component pads.
- **dts0100428972** — Traces can be deleted when Expedition is closed and reopened on very large designs with millions of user layer graphics objects.
- **dts0100505928** — ccz file does not contain trace information when plane shape is hatched
- **dts0100548186** — Expedition PCB can crash when DiffPairs are defined for nets with Duplicate pin numbers defined within Cell.
- **dts0100588961** — Dynamic Planes: The result of dynamic plane, some clearances used are bigger than the rule value.
- **dts0100590548** — Jumpers: Jumper is inserted on wrong side of the board during plow
- **dts0100594613** — Documentation: Need to explaining how to use escape options in BGA fanout dialog.
- **dts0100597013** — Dynamic Planes: Plowing from/to plane creates short circuit between vias and ground plane
- **dts0100598196** — Padstack Technology is not in CCZ file
- **dts0100599779** — Both Plated and Un-plated Contours appear Plated in the ODB++ (Valor)
- **dts0100606323** — gerber output (Remove Unused Pads Option) is removing pads it should not remove
- **dts0100607669** — Dynamic Planes: Short to positive dynamic plane to square pad with rounded corners.
- **dts0100608017** — Padstack Processor: Out of Memory error for Padstack Processing on large designs with user layer pads.
- **dts0100608660** — Layer Overrides of Pads in Padstack Editor on a userdraft Layer won't get outputted to .cc and .ccz file
- **dts0100608874** — Expedition PCB can crash when DiffPairs are defined for nets with Duplicate pin numbers defined within Cell.
- **dts0100611188** — Documentation: Resistor Shape's view is associated with Plane shape in Display Control. Customer request this info to be added in Help Topics for Resistor Shape
- **dts0100615378** — ODB++ output is causing circular objects on plane layer.

- **dts0100616375** — There are components missing in the CCZ file after direct export from Expedition.
- **dts0100616634** — Setup Parameters: ExpPCB can crash when choosing a Via Definitions tab after having chosen an Apply button.
- **dts0100619044** — Expedition PCB can crash when DiffPairs are defined for nets with Duplicate pin numbers defined within Cell.
- **dts0100621108** — Review Hazards: Report All PCB Hazards can cause software crash with accepted hazards that no longer exist in design.
- **dts0100622635** — Automation: ExpPCB - Script crashes Expedition when the stop button from the Open Script form is pressed
- **dts0100623940** — CCZ file generated by EE2007.6 has some major issues
- **dts0100627958** — Tuning: Design can crash when a tune is done with Arc's and specific Min Height.
- **dts0100628495** — Dynamic Planes: Vias of one signal are buried in plane of a different signal
- **dts0100628779** — DFT Access Analysis not correctly calculating exposed metal on bottom surface - no access!
- **dts0100629630** — Dynamic Teardrops: Expedition can crash while processing teardrops on all through pads with specific settings.
- **dts0100631836** — ODBG Interface is not processing Users Layers.
- **dts0100633828** — Place Via: Expedition PCB can crash on LMB click after selecting via in layout with Place Via dialog open
- **dts0100633852** — CMC: Using keyin command can crash Expedition PCB while trying to move circuit.
- **dts0100635966** — ODBG interface is failing to output User Layers.
- **dts0100635743** — XtremePCB: Once Tune is done on a group of nets, it the Client goes out of sync.

Known Problems and Workarounds

- **dts0100324957** — EXP PCB design with Detailed View and Display Control menu open will crash application when running Print preview.

  Workaround: Close Display Control before running print preview.
- **dts0100339520** — Expedition startup: Crash during startup on 2005Sp1. Crash during reload on 2005.05 during Forward annotation. Caused by a plane shape on layer 0. Limited number of designs affected.

Workaround: Export the Design to HKP and manually remove or edit the layer 0 objects to a valid layer.

- **dts0100408323** — Crash when importing EDIF Netlist. EDIF Netlist import crashes when very long name is used for design or cell

  Workaround: Modify the long cell or design names within EDIF Netlist before importing.

- **dts0100436731** — Expedition PCB crashes on load with 2005.1 NC/NP design being run in 2007. It was determined that this design was crashing because it ran out of memory during load.

  Workaround: If you setup the machine to use 3GB of RAM it will open. Also, if you delete the 32 MB GenDataDB.gdt or turn off dynamic planes it will load.

- **dts0100441244** — DFL Mode - Crash occurs while autorouter is running. Differential pair net definitions are wrong in the design.

  Workaround: Correct differential pair net names before creating Expedition files.

- **dts0100459782** — Expedition crashes when trying to subtract text from draw object.

  Workaround: Don't subtract text from draw object.

- **dts0100469174** — Renaming the schematic in DxD cause error in Expedition.

  Workaround: Run FA from the status bar the first time after renaming the root schematic, and then subsequently run FA from the PI dialog. Other lower-level blocks can be renamed and FA successfully run from the PI dialog.

- **dts0100465266** — Help menu entries that link to Supportnet cannot get past the login screen (the mfcie browser seems to hang)

  Workaround: Use a standalone browser

- **dts0100504881** — OpenGL: the screen is not refreshed correctly when using Remote Desktop

  Workaround: OpenGL is not supported with remote displays on any platform. This includes Remote Desktop on Windows and remote displays on UNIX and Linux. The work-around for this is to use the display directly connected to the computer rather than a remote connection.

- **dts0100515390** — Forward Annotation failed with simple project with Logical Physical Reuse Block

  Workaround: Create the vias first before FA.

- **dts0100517339** — EGS OpenGL does not display correctly from remote Linux machine

  Workaround: OpenGL is not supported with remote displays on any platform. This includes Remote Desktop on Windows and remote displays on UNIX and Linux. The work-around for this is to use the display directly connected to the computer rather than a remote connection.

- **dts0100568836** —Variant data is not generated when the option, FablinkXE data generation mode is selected as On Exit.

  Workaround: Use FablinkXE variant data generation mode "On Save" or "By User's Request"

- **dts0100569838** — crash on exit due to testpoints with missing pins

  Workaround: Design can be fixed by resetting cells

- **dts0100013914** — Package cell won't display in PDB preview window if it contains a nested mechanical or drawing cell

- **dts0100016764** — Move Part cleanup of connected traces used Gloss Settings

- **dts0100017842** — Ascii out PDB and the units are set to "th" no matter the units in PDB

- **dts0100157287** — Teardrops connected to Net0 or Net0-X are not outputted to gerber

- **dts0100157420** — Reuse Blocks do not support instantiated padstack or cell changes being replicated once placed in design.

- **dts0100284023** — Alt key for Plow Multiplow on a diff pair is not working on Linux

  Workaround: The workaround is to delete this hot key. Go to Program->Settings->Desktop->Window Manager and run the configuration. In the bindings section, you can change/delete the hotkey settings.

- **dts0100442708** — RB Cell can not have more layers than target design. Currently it issues an error... "Reusable Block cannot have more layers than the Target design."

- **dts0100454666** — Do not support TeamPCB in Undocked designs. Dock causes data to be lost when Undocked design was split and edited using TeamPCB.

- **dts0100458494** — DxD prevent FA or BA option changes are not seen in XtremePCB while up

- **dts0100463398** — Save no longer automatically runs Back Annotation in 2007.

  Workaround: Small script can have the Save operation automatically run Back Annotation.

- **dts0100494254** — IDF for designs with RBs do not contain all component information

  Workaround: Open Design, Flatten RB Cells and create IDF output. Then Exit without saving.

- **dts0100524570** — Batch DRC is flagging a Electrical DiffPair trace to diff pair trace violation where the Cross Class Clearance rules are correct.

  Workaround: Change to physical nets instead of electrical nets in CES.

- **dts0100533325** — Review Hazards Accept does not work for Online->Differential pairs->Convergence hazards

- **dts0100533326** – Review Hazards Accept does not work for Online->Differential pairs->Convergence Tolerance hazards
- **dts0100552197** — Sometimes a machine can crash when opening a design that needs to be migrated between releases.

  Workaround: Remove Windows Services for UNIX
- **dts0100565368** — Fiducials and Test Points within Cavities can have incorrect layer color in top-facing cavity
- **dts0100567395** – Changing Root Block in Dx can cause errors when ExpPCB is launched from Dx.

  Workaround — Go back to the original design instead of using the new design created by launching Expedition from DxDesigner
- **dts0100571571** – Errors during TeamPCB join process when Advanced Packaging bond wires and pads are added to split design.
- **dts0100582670** — Do not support All to All for Estimated Crosstalk definitions within CES. Review Hazards will not report violations.

  Workaround: Define the rules by net or netclass.
- **dts0100583405** — Automatic Pad Growing modifications of padstacks are not propagated when a circuit is copied with CMC.
- **dts0100583448** — Automatic Pad Growing if the Padstack Processor is used to change connected pad to a padstack with NC No Pad. Padstack updates but no longer have automatic growing.
- **dts0100592821** — When a meander is terminated with a via using the add meander command and the command is terminated, will it not be possible to continue from the via with a new meander on a different layer.

  Workaround: If this is the desired behavior should a standalone via be used instead.
- **dts0100592843** — Jumpers placed on the board are getting messed up after opening cell's properties in Cell Editor.
- **dts0100596968** — Custom layer names in CES stackup editor are overwritten when adding layers via Setup Parameters.
- **dts0100597098** — Forward Annotation Netload process crashes when a schematic contains parts with no net connections or augmented PDB nets.
- **dts0100600581** — Set via span definition from Laminate to Buildup can crash application

  Workaround: Export JobPrefs HKP from within Expedition PCB. Exit and compile this exported file using hkp2jobprefsdb to synchronize stackups.
- **dts0100601534** — Cross probe between CES and ExpPCB with Review Hazards has big performance hit.

Workaround: Close Review Hazards and use the CES Actuals.

- **dts0100603832** — DC Reuse assignment of different Ref Des on RB and package in DC, all nets will be assigned to Net0 after 1st Forward Annotation

  Workaround: Run Forward Annotation a 2nd time to have the correct nets assigned to the Reuse Block.

- **dts0100606077** — If the values to create a draw object are entered into the properties window you can not click off of the object.

  Workaround: Use RMB cancel option to exit selection of object.

- **dts0100606281** — Automatic Pad Growing changing to an alternate technology in Setup Parms doesn't update net 0 pins with new NC/Override rules. No hazards reported...

  Workaround: Do a reset cell to have the pads correctly defined.

- **dts0100606947** — Xtreme a crash can occur when you have Copied Traces in Dynamics and you toggle DRC Teardrops/Breakouts as Traces or Pads

Chapter 6
FabLinkXE

Problems Fixed

- **dts0100599537** — Dimensioning not possible in Drawing Editor
- **dts0100620701** — FLXE export CCZ: If Smart Utilities is installed, Fablink place design and fablink export CCZ crashes the child process (fablinkxe.exe) and leaves the process running in background.
- **dts0100635020** — After putting the update design with FablinkXE,the Expedition data becomes read-only.

Known Problems and Workarounds

- **dts0100453808** — EVM: The FXE data generated doesn't get deleted if we try to choose different variants while generating FXE Data

  Workaround : User can manually delete the <varaint_name>.lyt file from FLXE_varaint_data folder

- **dts0100496447** — DE :layerstackup representation is not correct in Drawing Editor

  Workaround : User can manually edit the text in layer stackup as required

Chapter 7
HyperLynx Analog

Problems Fixed

- **dts0100616119** — .option tuning will override user value for eps

Known Problems and Workarounds

- **dts0100567491** — [Linux] Compilation fails for projects in paths with spaces

  Workaround: Use projects in paths without spaces, or use symbolic links for the projects with spaces in this case (This should be fixed in AMS2009.1)

- **dts0100566280** — Simulating using HLA does not work when installed in a non standard path which contains a space

  Workaround: Install HyperLynx Analog in any path without spaces.

- **dts0100574753** — Switch is ignored by hyperlynx analog simulator

  Workaround: Add a large resistor between the V+ control pin and ground

Chapter 8
I/O Designer

Problems Fixed

- **dts0100368440** — IO standard has not been removed from ucf.
- **dts0100491672** — IOD crashes with PROLOG SYSTEM ERROR when unraveling nets in device view
- **dts0100602206** — IOD not outputting good Actel PDC file
- **dts0100614926** — Please add support for ISE 11.2 library.
- **dts0100616172** — IOD needs to support the Spartan 6 devices.
- **dts0100620449** — Duplicated signals after importing from HDL and QSF
- **dts0100621902** — Database Settings not prompted when loading FPC.
- **dts0100625292** — Pin swaps are not imported
- **dts0100626736** — Environment variable in .prj file not supported
- **dts0100629113** — Unravel of crossover nets is broken. Immediate fix needed.
- **dts0100632195** — Schematic Update is removing and not adding any power, ground and/or config pins defined as signals and/or added to the PCB symbols in the DxD schematic.
- **dts0100632619** — Cannot assign output IO signal

Chapter 9
ICX Pro Explorer

Problems Fixed

- **dts0100620480** — Simulation has incorrect levels when "enabling" the model - when you disable it simulations are probably correct - when a model is disabled it should not be used for simulations. GUI is broken.

Chapter 10
ICX Pro Verify

Known Problems and Workarounds

- **dts0100635571** — no Verify hazard for violated simulated min delay actual.

  Workaround: the erroneous value can be read out in the verify Delay Summary hazard
- **dts0100623064** — ICX Pro Verify standalone can't open keyin-netlist design

  Workaround: open design in ExpeditionPCB with ICX Pro Verify license enabled

Chapter 11
Installation

Problems Fixed

- **dts0100607616** — During testing of EE7.5 Update 6 and 7, we received a error about post_install_script.bat

Chapter 12
Library Manager

Problems Fixed

- **dts0100570415** — Changing 'User Defined Layer' on one Cell will reflect on another Cell.
- **dts0100608412** — Edits don't save to database when made in Library Manager.

Known Problems and Workarounds

- **dts0100002473** — If you try to move a symbol into a library that has the potential of being "full" or is "full", it will fail an import and delete the symbol instead of failing import and leaving the symbol in the original base Central Library or symbol library (*.slb) file.

  Workaround: Create and use multiple symbol partitions. Do not store all symbols in a single symbol partition.

- **dts0100018307** — ASCII Import of Parts should have option to overwrite existing data in library, regardless of TIMESTAMP

  Workaround: Delete the time stamp information for each object in the HKP file.

- **dts0100155914** — When using Library Services, the Import HKP command ignored some draw objects on the solderpaste layer. No error or warning message displays. However, the log file displays the information that was omitted from the design.

  Workaround: Ensure that all solderpaste objects in a cell are closed shapes (for example, rectangles, polygons, and so forth) to avoid this problem.

- **dts0100195212** — Linux DxD FLow: Pad descriptions not aligned with Pad fields - remote display

  Workaround: Use local display if necessary.

- **dts0100330431** — Signal Vision / Signal Analyser checkbox is grayed out but CHECKED in case of DxD library

  Workaround: Temporarily change the FlowType key in the CL's .cfg file from "DX" to "DC"; Open LM and unCheck the box, Close LM, change the FlowType key back to "DX".

- **dts0100395519** — Vertical coordinates entered in tcl commands seem to be mirrored

  Workaround: Normally, Positive coordinates entered are to the right or above the origin, and negative coordinates are to the left or below the origin, depending upon X or Y axis.. When using the Dx Symbol Editor API, these coordinates are reversed.

- **dts0100415649** — Parts and Cells used in UnVerified ReUse blocks can be deleted from the CL. An error should be issued (as currently done with Verified RBs).

  Workaround: None, except ensure that all Reuse Blocks are Verified before deleting any parts and cells from the Central Library.

- **dts0100436048** — Symbol preview is empty for symbol of name containing spaces.

  Workaround: Ensure symbol names do not contain spaces.

- **dts0100436049** — Symbol copy and symbol rename functions don't allow symbol name with space(s).

  Workaround: Ensure symbol names do not contain spaces.

- **dts0100442194** — Cannot define implicit and explicit power pins in PDB Editor and cannot package

  Workaround: Power pins for a given part must either be defined as implicit or explicit, but not both.

- **dts0100453024** — Error changing DC flow LT to "CES Enabled": "Unable to access the LogicDB at Work\Layout_Temp\LogicDB.lgc"

  Workaround: Ignore the error message.

- **dts0100459897** — DC Reuse: FA Error attempting to Migrate UnVerified (without RB cell) CES-enabled DC-flow RB .

  Workaround: Manually enable CES for Reuse Designs after migration.

- **dts0100460114** — Dx Reuse: Plane definition is lost after FA during Reuse Verification.

  Workaround: Re-define the Plane definition when Reuse Block is placed in the Host design.

- **dts0100461393** — The system allow to create a DxD symbol name with a . (dot) character but then there is no way to select it.

  Workaround: Do not include . (dot) in symbol names.

- **dts0100461487** — Error attempting to save Dx symbols on Linux (RH4, update 2): "Error executing: /data/trees/2007.1/2007EE/SDD_HOME/lm/linux/dxlib2lmc ..."

  Workaround: Either ignore the error, or upgrade to RedHat 4, update 3 or higher.

- **dts0100462611** — Receiving Segmentation Fault on Solaris when Accessing help on Visual IBIS Editor in Library Manager

  Workaround: Establish a default web browser. Its only a problem if Web browser has not been established/defined.

- **dts0100465539** — The Layout Templates included in the sample Central Library delivered by EE2007.2 will not open - They are missing the keyin.icdb folder and the CL pointer in the Layout Templates project file is wrong.

Workaround: Create a new Central Library ; Copy the keyin.icdb folder from the new Central Library's Layout Templates into the Layout Templates in the Sample CL (make sure to copy the 4 layer into the 4 layer, and 8 layer into the 8 layer). Also, edit the project file in both of the Layout Templates and change the Central Library name to SampleLib.lmc.

- **dts0100466625** — Missing pins during import pins in Symbol Editor

  Workaround: Ensure pin names are unique in the .CSV file. If the .CSV file contains multiple pins with the same Pin Name, only the last pin is imported

- **dts0100466734** — Some Dx symbols in the testcase CL do not preview in Nav Tree or Part Editor, but open OK in NSE.

  Workaround: Either remove the lib.cfg file (located under the symbol partition), or change the alias in the file to the correct partition name. The preference is to delete the file, since the alias would have to be manually changed whenever (if) the partition is renamed. It was also noticed that symbols in the builtin partition were defined in mega-file format, which is not supported in EE2007.2 release.

- **dts0100489429** — In the RB editor, Save RB function looks at the iCDB snapshot in the Back-end when checking to see if all instance data is absorbed

  Workaround: Run FA again after Absorbing the schematic data and then Save (Verify) will complete OK.

- **dts0100498141** — Help for DC flow Symbol Editor doesn't work on VISTA

  Workaround: The Vista customer can download the WinHlp32.exe from Microsoft website.

- **dts0100498548** — Error when opening a DC-flow CL when only DC-flow LM is installed: "WDIR EV doesn't contain %SDD_HOME%\standard path."

  Workaround: Add the following path to the WDIR variable:

  C:\Mentor_2007\2007EE\SDD_HOME\standard

  If DC is also installed, the path is added automatically so the workaround is not necessary.

- **dts0100561271** — "Global Signal Name" written back to ASCII symbol file not NETNAME

  Workaround: If backward compatibility to 2005.x is required:

  Modify the global symbols to use NETNAME instead of Global Signal Name.

  Map NETNAME to "Global Signal Name" in the map.cfg file on 2007.5 workstation.

- **dts0100541685** — I get iCDBError in NSE if tried to Edit Block Symbol on Logical Physical Reuse Block

  Workaround: Remove the sAddress.adr file, under the __ReusableBlocksSymb folder. This is a temporary file that is normally removed, but can remain if the iCDB server crashes or the process is killed for some other reason.

- **dts0100504212** — Crash of NSE while opening symbol with bitmap.

  Workaround: Bitmaps are not supported on solaris. The workaround how to open symbol without crash and without bitmap is to delete the content of ole directory (delete the information about bitmap) under the partition folder in CL, i.e. $CL/SymbolLibs/builtin/ole

- **dts0100562047** — Incompatibility with 2007 libraries

  Workaround: After migrating the CL to 2007.5, edit the Centlib .prp file and change the Version from 16 to 15 (at the end of the Comments section).

- **dts0100595779** — Error creating RB with design open, but doesn't say what the problem is and doesn't create a log file.

  Workaround: Ensure the source design is not open before using it to create a new Reuse Block.

Chapter 13
Smart Utilities

Problems Fixed

- **dts0100623360** — Application error occured by using the Cut of FatTraceEdit.

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